



Substitute for form 1449B/PTO		<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		Application Number	10/057,637
		Filing Date	January 24, 2002
		First Named Inventor	Yatin Hoskote
		Art Unit	2124
		Examiner Name	Tan V. Mai
		Attorney Docket Number	2207/12793
Sheet		of	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
man		H. Suzuki et al, "Leading Zero Anticipatory Logic for High Speed Floating Point Addition", IEEE Journal of Solid-State Circuits, Vol 31, No. 8, Aug. 1996 pp. 1157-1164	
↓		K.T. Lee and K.J. Nowka, "1Ghz Leading Zero Anticipator Using Independent Sign-Bit Determination Logic", 2000 Symposium on VLSI Circuits Digest of Technical Papers, pp. 194-195	
↓		E. Hokenek et al, "Second Generation RISC Floating Point with Multiply-Add Fused", IEEE Journal on Solid-State Circuits, Vol. 25, No. 5, Oct. 1990, pp. 1207-1213	

Examiner Signature	man	Date Considered	3/2005
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

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